

ASSP For Power Supply Applications

Power Voltage Monitoring IC with Watchdog Timer

MB3793-30A

DESCRIPTION

The MB3793 is an integrated circuit to monitor power voltage; it incorporates a watchdog timer.

A reset signal is output when the power is cut or falls abruptly. When the power recovers normally after resetting, a power-on reset signal is output to microprocessor units (MPUs). An internal watchdog timer with two inputs for system operation diagnosis can provide a fail-safe function for various application systems.

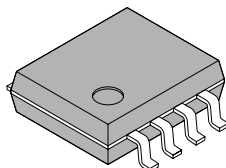
There is also a mask option that can detect voltages of 4.9 V to 2.4 V in 0.1-V steps.

FEATURES

- Precise detection of power voltage fall: $\pm 2.5\%$
- Detection voltage with hysteresis
- Low power dispersion: $I_{CC} = 31 \mu\text{A}$ (reference)
- Internal dual-input watchdog timer
- Watchdog-timer halt function (by inhibition pin)
- Independently-set watchdog and reset times

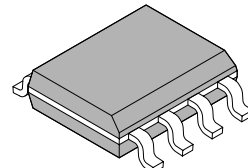
PACKAGE

8-pin, Plastic SOP



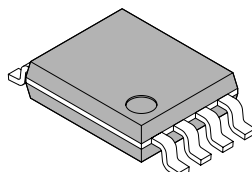
(FPT-8P-M01)

8-pin, Plastic SOL



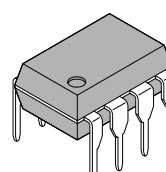
(FPT-8P-M02)

8-pin, Plastic SSOP



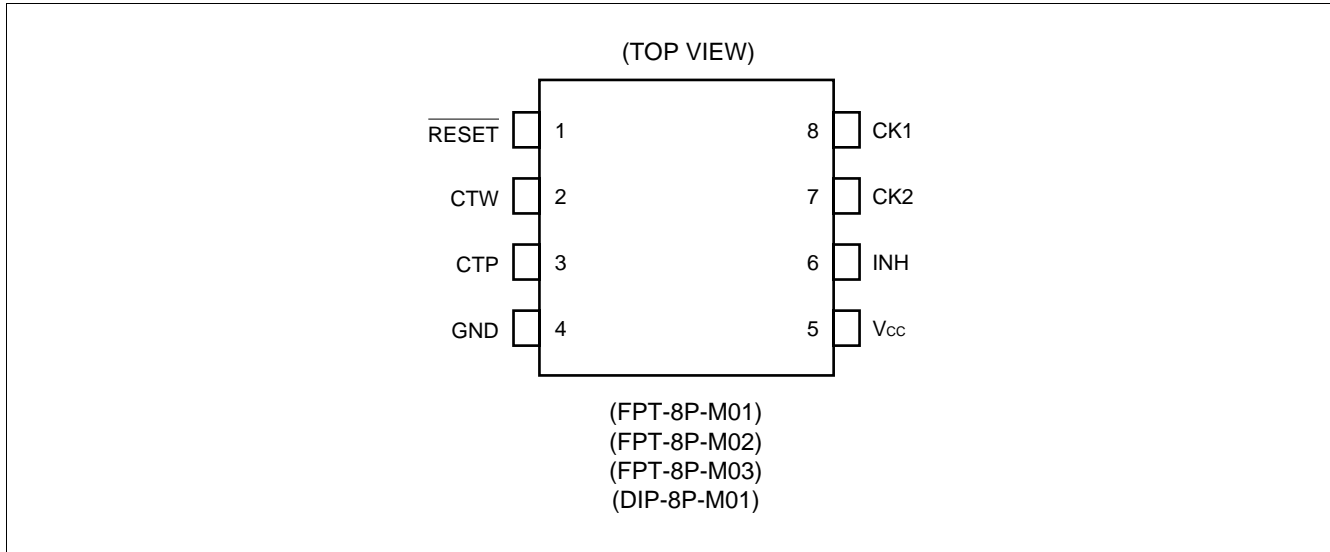
(FPT-8P-M03)

8-pin, Plastic DIP



(DIT-8P-M01)

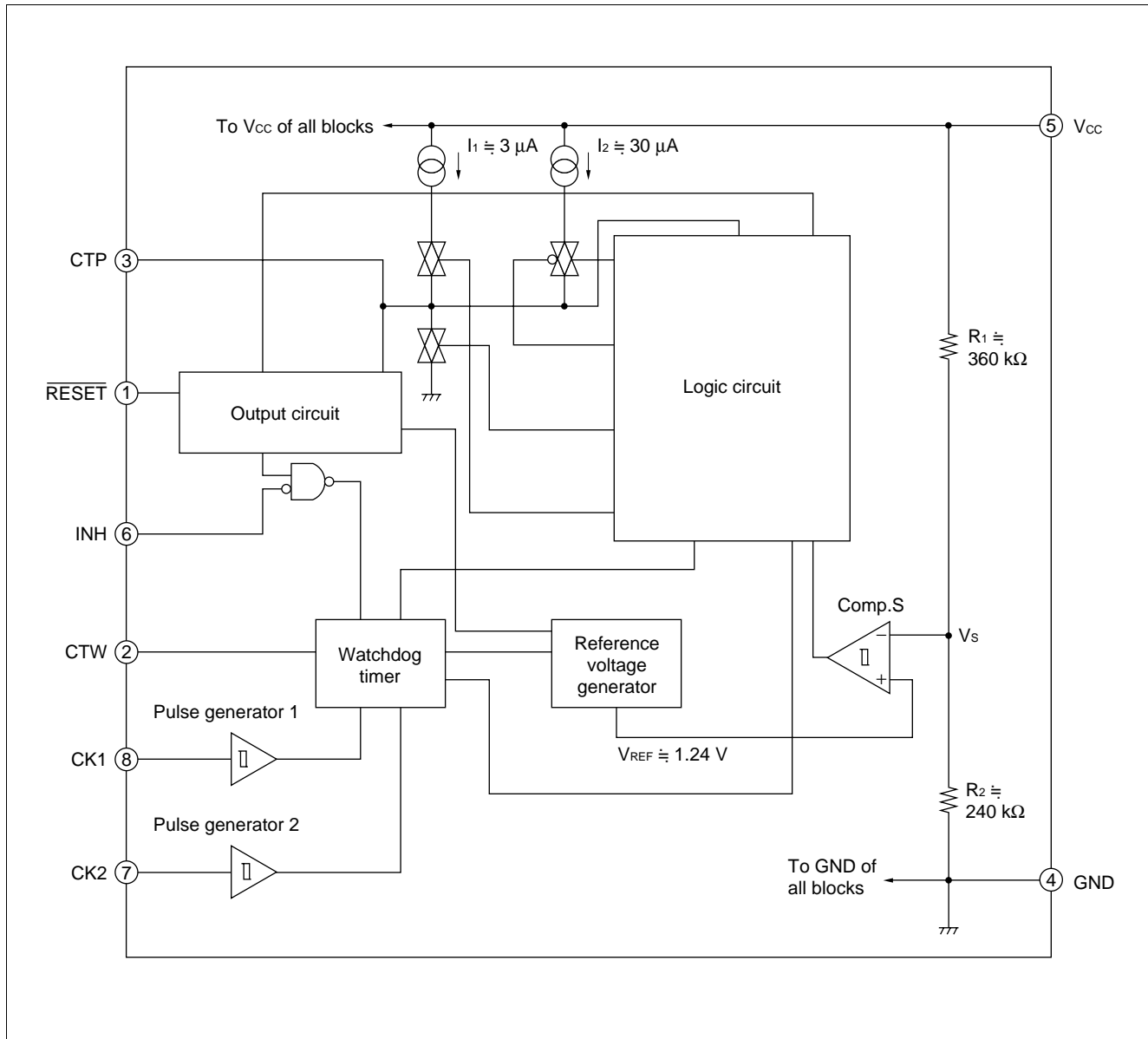
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Symbol	Descriptions	Pin no.	Symbol	Descriptions
1	$\overline{\text{RESET}}$	Outputs reset pin	5	V _{cc}	Power supply pin
2	CTW	Watchdog timer monitor time setting pin	6	INH	Inhibit pin
3	CTP	Power-on reset hold time setting pin	7	CK2	Inputs clock 2 pin
4	GND	Ground pin	8	CK1	Inputs clock 1 pin

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

1. Comp. S

Comp. S is a comparator with hysteresis to compare the reference voltage with a voltage (V_s) that is the result of dividing the power voltage (V_{CC}) by resistors 1 and 2. When V_s falls below 1.24 V, a reset signal is output. This function enables the MB3793 to detect an abnormality when the power is cut or falls abruptly.

2. Output circuit

The output circuit contains a $\overline{\text{RESET}}$ output control comparator that compares the voltage at the CTP pin to the threshold voltage to release the $\overline{\text{RESET}}$ output if the CTP pin voltage exceeds the threshold value.

Since the reset ($\overline{\text{RESET}}$) output buffer has CMOS organization, no pull-up resistor is needed.

3. Pulse generator

The pulse generator generates pulses when the voltage at the CK1 and CK2 clock pins changes to High from Low level (positive-edge trigger) and exceeds the threshold voltage; it sends the clock signal to the watchdog timer.

4. Watchdog timer

The watchdog timer can monitor two clock pulses. Short-circuit the CK1 and CK2 clock pins to monitor a single clock pulse.

5. Inhibition pin

The inhibition (INH) pin forces the watchdog timer on/off. When this pin is High level, the watchdog timer is stopped.

6. Logic circuit

The logic circuit contains flip-flops.

Flip-flop RSFF1 controls the charging and discharging of the power-on reset time setting capacitor (C_{TP}).

Flip-flop RSFF2 turns on/off the circuit that accelerates charging of the power-on reset time setting capacitor (C_{TP}) at a reset. The RSFF2 operates only at a reset; it does not operate at a power-on reset when the power is turned on.

■ ABSOLUTE MAXIMUM RATINGS

(Ta = +25 °C)

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power supply voltage*	V _{CC}	—	-0.3	+7	V
Input voltage*	CK1	V _{CK1}	-0.3	V _{CC} + 0.3 (≤ +7)	V
	CK2	V _{CK2}			
	INH	I _{INH}			
Reset output voltage*	$\overline{\text{RESET}}$	V _{OL} V _{OH}	-0.3	V _{CC} + 0.3 (≤ +7)	V
Reset output current		I _{OL} I _{OH}			
Power dissipation	P _D	Ta ≤ +85 °C	—	200	mW
Storage temperature	T _{stg}	—	-55	+125	°C

* : The voltage is based on the ground voltage (0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply voltage	V _{CC}	—	1.2	3.3	6.0	V
Reset ($\overline{\text{RESET}}$) output current	I _{OL}	—	0	—	+5	mA
	I _{OH}	—	-5	—	0	
Power-on reset hold time setting capacity	C _{TP}	—	0.001	0.1	10	μF
Watchdog-timer monitoring time setting capacity*	C _{TW}	—	0.001	0.01	1	μF
Operating temperature	Ta	—	-40	+25	+85	°C

* : The watchdog timer monitor time range depends on the rating of the setting capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{CC} = +3.3 V, T_a = +25 °C)

Parameter	Symbol	Conditions	Value			Unit	
			Min	Typ	Max		
Power supply current	I _{CC1}	After exit from reset	—	31	45	μA	
Detection voltage	V _{SL}	V _{CC} falling	T _a = +25 °C	2.93	3.00	3.07	V
			T _a = -40 °C to +85 °C	(2.89)*	3.00	(3.11)*	
	V _{SH}	V _{CC} rising	T _a = +25 °C	3.00	3.07	3.14	V
			T _a = -40 °C to +85 °C	(2.96)*	3.07	(3.18)*	
Detection voltage hysteresis difference	V _{SHYS}	V _{SH} - V _{SL}	30	70	110	mV	
Clock-input threshold voltage	V _{CIH}	CK rising	(0.7)*	1.3	1.9	V	
	V _{CIL}	CK falling	0.5	1.0	(1.5)*	V	
Clock-input hysteresis	V _{CHYS}	—	(0.1)*	0.3	(0.6)*	V	
Inhibition-input voltage	V _{I_{IH}}	—	2.2	—	V _{CC}	V	
	V _{I_{IL}}	—	0	—	0.8		
Input current (CK1, CK2, INH)	I _{IH}	V _{CK} = 5 V	—	0	1.0	μA	
	I _{IL}	V _{CK} = 0 V	-1.0	0	—	μA	
Reset output voltage	V _{OH}	I _{RESET} = -3 mA	2.8	3.10	—	V	
	V _{OL}	I _{RESET} = +3 mA	—	0.12	0.4	V	
Reset-output minimum power voltage	V _{CCL}	I _{RESET} = +50 μA	—	0.8	1.2	V	

* : The values enclosed in parentheses () are setting assurance values.

2. AC Characteristics

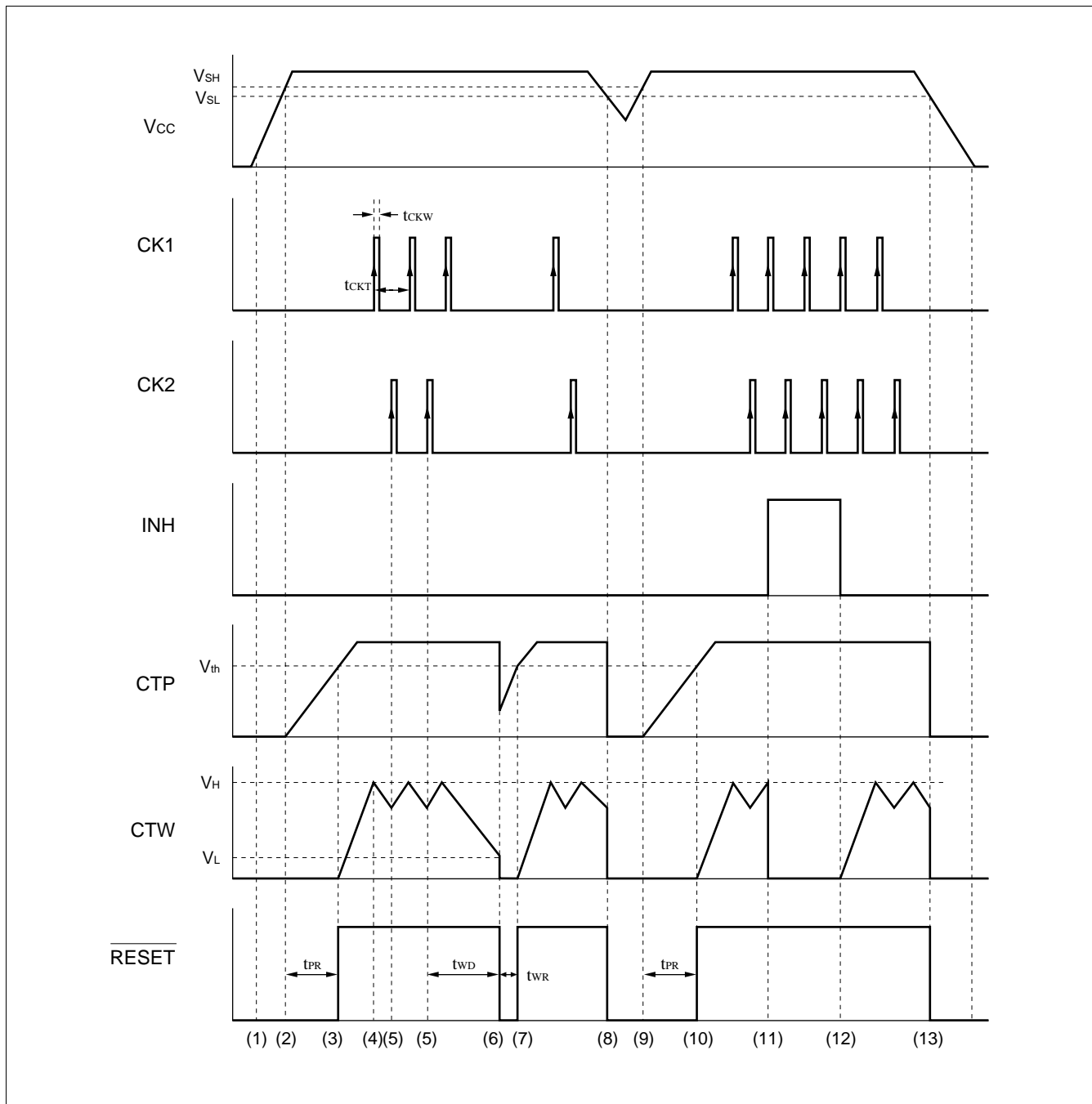
(V_{CC} = +3.3 V, T_a = +25 °C)

Parameter	Symbol	Conditions	Value			Unit	
			Min	Typ	Max		
Power-on reset hold time	t _{PR}	C _{TP} = 0.1 μF	30	75	120	ms	
Watchdog timer monitor time	t _{WD}	C _{TW} = 0.01 μF, C _{TP} = 0.1 μF	8	16	24	ms	
Watchdog timer reset time	t _{WR}	C _{TP} = 0.1 μF	2	5.5	9	ms	
Clock input pulse width	t _{CKW}	—	500	—	—	ns	
Clock input pulse cycle	t _{CKT}	—	20	—	—	μs	
Reset ($\overline{\text{RESET}}$) output transition time	Rising	t _r *	C _L = 50 pF	—	—	500	ns
	Falling	t _r *	C _L = 50 pF	—	—	500	ns

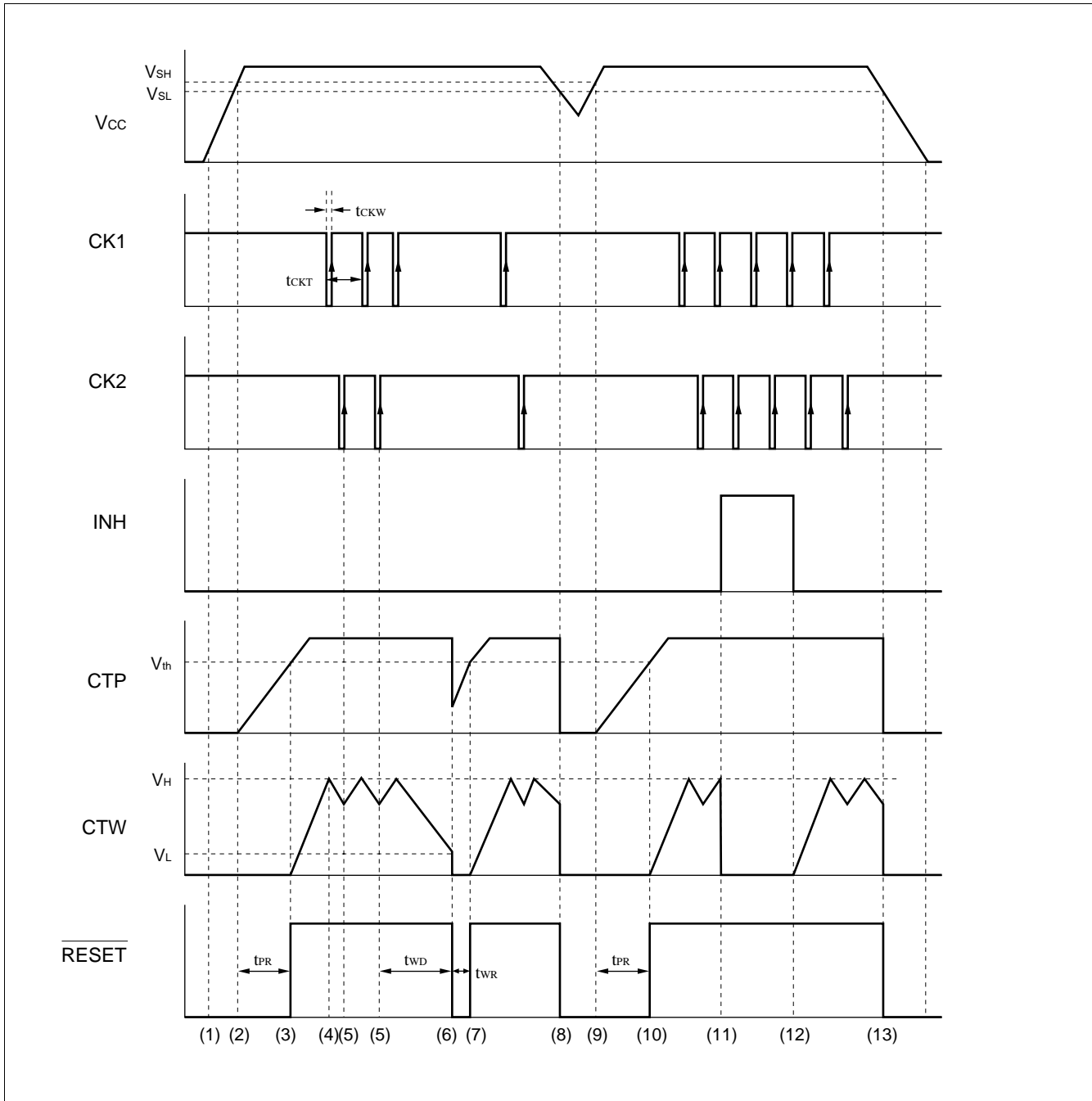
* : The voltage range is 10% to 90% at testing the reset output transition time.

■ DIAGRAM

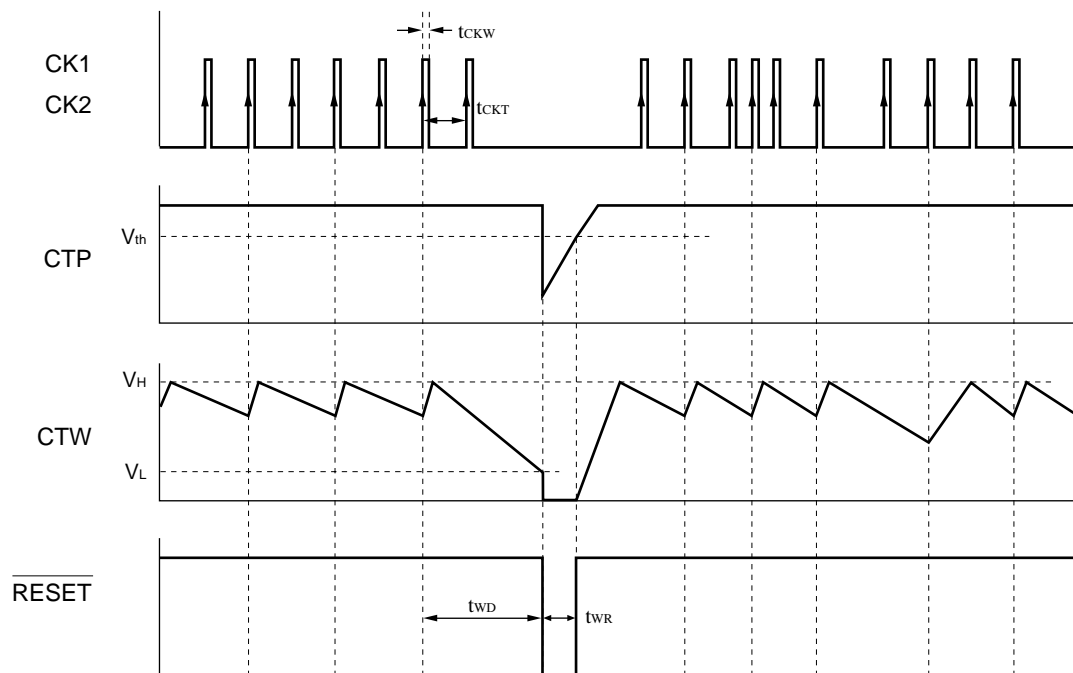
1. Basic operation (Positive clock pulse)



2. Basic operation (Negative clock pulse)

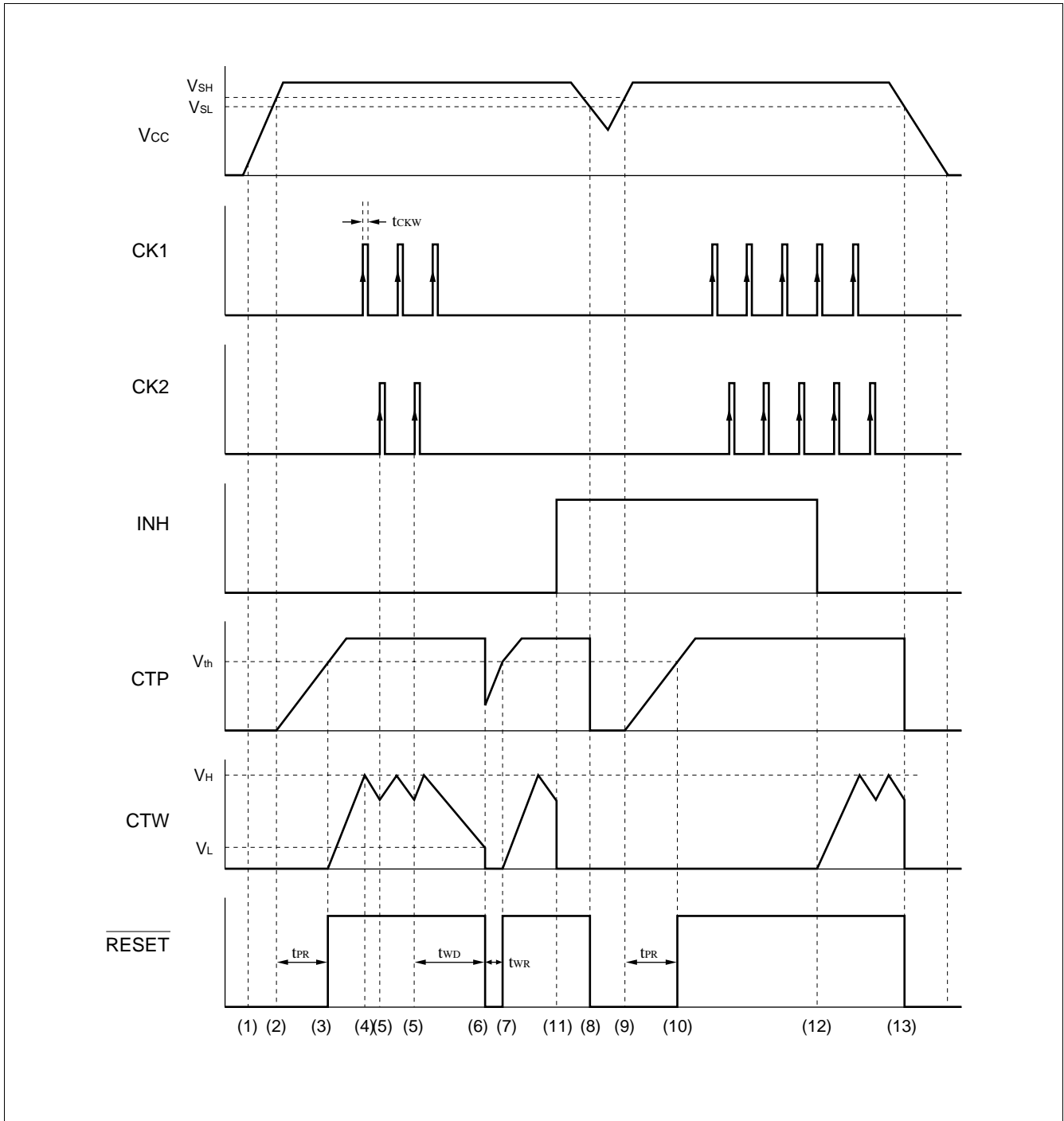


3. Single-clock input monitoring (Positive clock pulse)

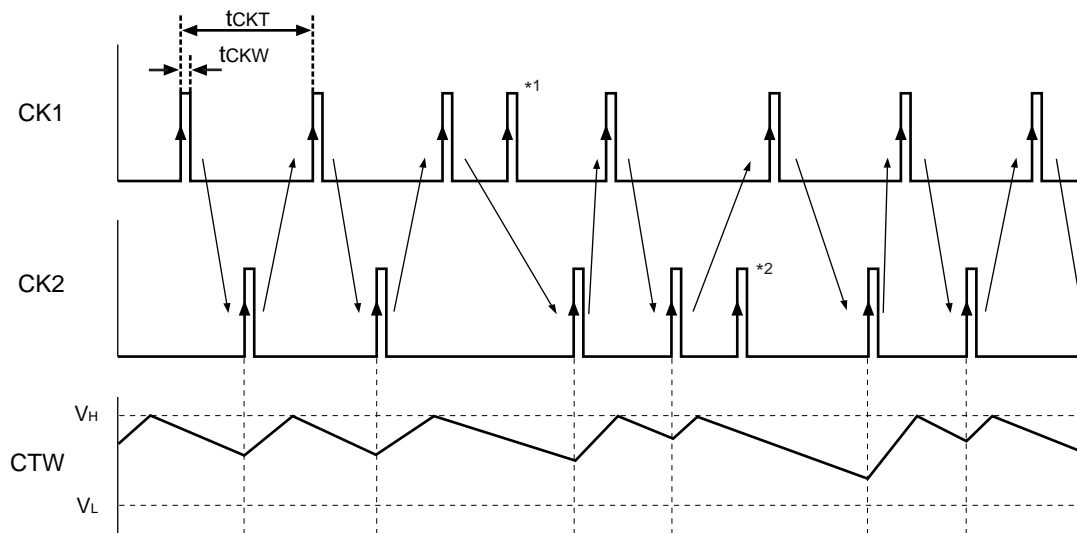


Note : The MB3793 can monitor only one clock.
 The MB3793 checks the clock signal at every other input pulse.
 Therefore, set watchdog timer monitor time t_{WD} to the time that allows the MB3793 to monitor the period twice as long as the input clock pulse.

4. Inhibition operation (Positive clock pulse)



5. Clock pulse input supplementation (Positive clock pulse)



Note : The MB3793 watchdog timer monitors Clock1 (CK1) and Clock2 (CK2) pulses alternately.
 When a CK2 pulse is detected after detecting a CK1 pulse, the monitoring time setting capacity (C_{TW}) switches to charging from discharging.
 When two consecutive pulses occur on one side of this alternation before switching, the second pulse is ignored.
 In the above figure, pulse *1 and *2 are ignored.

■ OPERATION SEQUENCE

1. Positive clock pulse input

See “1. Basic operation (positive clock pulse)” under “■ DIAGRAM.”

2. Negative clock pulse input

See “2. Basic operation (negative clock pulse)” under “■ DIAGRAM.”

The MB3793 operates in the same way whether it inputs positive or negative pulses.

3. Clock monitoring

To use the MB3793 while monitoring only one clock, connect clock pins CK1 and CK2.

Although the MB3793 operates basically in the same way as when monitoring two clocks, it monitors the clock signal at every other input pulse.

See “3. Single-clock input monitoring (positive clock pulse)” under “■ DIAGRAM.”

4. Description of Operations

The numbers given to the following items correspond to numbers (1) to (13) used in “■ DIAGRAM.”

- (1) The MB3793 outputs a reset signal when the supply voltage (V_{CC}) reaches about 0.8 V (V_{CCL})
- (2) If V_{CC} reaches or exceeds the rise-time detected voltage V_{SH} , the MB3793 starts charging the power-on reset hold time setting capacitor C_{TP} . At this time, the output remains in a reset state. The V_{SH} value is 3.07 V (Typ) .
- (3) When C_{TP} has been charged for a certain period of time T_{PR} (until the CTP pin voltage exceeds the threshold voltage (V_{th}) after the start of charging), the MB3793 cancels the reset (setting the \overline{RESET} pin to “H” level from “L” level).
The V_{th} value is about 2.4 V with $V_{CC} = 3.3$ V

The power-on reset hold timer monitor time t_{PR} is set with the following equation:

$$t_{PR} \text{ (ms)} \cong A \times C_{TP} \text{ (}\mu\text{F)}$$

The value of A is about 750 with $V_{CC} = 3.3$ V. The MB3793 also starts charging the watchdog timer monitor time setting capacitor (C_{TW}).

- (4) When the voltage at the watchdog timer monitor time setting pin C_{TW} reaches the “H” level threshold voltage V_H , the C_{TW} switches from the charge state to the discharge state.
The value of V_H is always about 1.24 V regardless of the detected voltage.
- (5) If the CK2 pin inputs a clock pulse (positive edge trigger) when the C_{TW} is being discharged in the CK1-CK2 order or simultaneously, the C_{TW} switches from the discharge state to the charge state.
The MB3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses with the system logic circuit operating normally.
- (6) If no clock pulse is fed to the CK1 or CK2 pin within the watchdog timer monitor time t_{WD} due to some problem with the system logic circuit, the C_{TW} pin is set to the “L” level threshold voltage V_L or less and the MB3793 outputs a reset signal (setting the \overline{RESET} pin to “L” level from “H” level).
The value of V_L is always about 0.24 V regardless of the detected voltage.

The watchdog timer monitor time t_{WD} is set with the following equation:

$$t_{WD} \text{ (ms)} \cong B \times C_{TW} \text{ (}\mu\text{F)}$$

The value of B is hardly affected by the power supply voltage; it is about 1600 with $V_{CC} = 3.3$ V.

(Continued)

(Continued)

- (7) When a certain period of time t_{WR} has passed (until the CTP pin voltage reaches or exceeds V_{th} again after recharging the C_{TP}), the MB3793 cancels the reset signal and starts operating the watchdog timer. The watchdog timer monitor reset time t_{WR} is set with the following equation:
 $t_{WR} \text{ (ms)} \cong D \times C_{TP} \text{ (}\mu\text{F)}$
 The value of D is 55 with $V_{CC} = 3.3 \text{ V}$.
 The MB3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses. If no clock pulse is input, the MB3793 repeats operations (6) and (7).
- (8) If V_{CC} is lowered to the fall-time detected voltage (V_{SL}) or less, the CTP pin voltage decreases and the MB3793 outputs a reset signal (setting the $\overline{\text{RESET}}$ pin to "L" level from "H" level).
 The value of V_{SL} is 3.0 V (Typ) .
- (9) When V_{CC} reaches or exceeds V_{SH} again, the MB3793 starts charging the C_{TP} .
- (10) When the CTP pin voltage reaches or exceeds V_{th} , the MB3793 cancels the reset and restarts operating the watchdog timer. It repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses.
- (11) Making the inhibit pin active (setting the INH pin to "H" from "L") forces the watchdog timer to stop operation.
 This stops only the watchdog timer, leaving the MB3793 monitoring V_{CC} (operations (8) to (10)).
 The watchdog timer remains inactive unless the inhibit input is canceled.
 The inhibition (INH) pin must be connecting a voltage of more low impedance, to evade of the noise.
- (12) Canceling the inhibit input (setting the INH pin to "L" from "H") restarts the watchdog timer.
- (13) The reset signal is output when the power supply is turned off to set V_{CC} to V_{SL} or less.

1. Equation of time-setting capacitances (C_{TP} and C_{TW}) and set time

$$t_{PR} \text{ [ms]} \cong A \times C_{TP} \text{ [}\mu\text{F]}$$

$$t_{WD} \text{ [ms]} \cong B \times C_{TW} \text{ [}\mu\text{F]}$$

$$t_{WR} \text{ [ms]} \cong D \times C_{TP} \text{ [}\mu\text{F]}$$

Values of A, B, C, and D

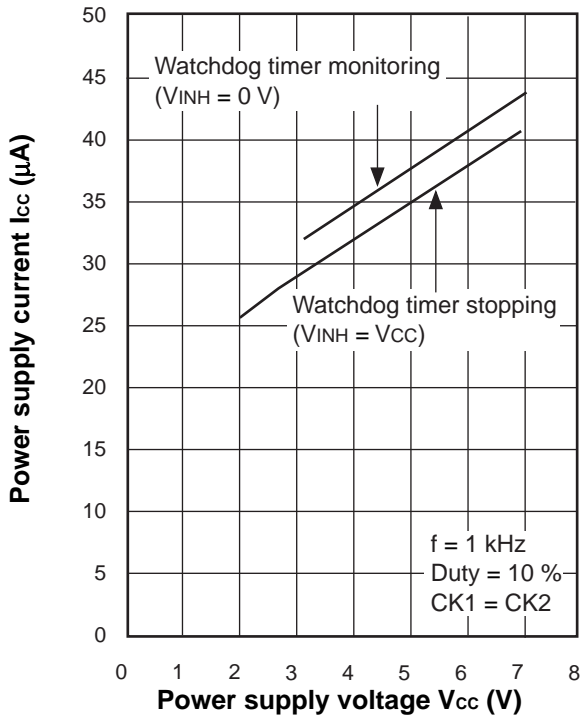
A	B	C	D	Remark
750	1600	0	55	$V_{CC} = 3.3 \text{ V}$
1300	1500	0	100	$V_{CC} = 5.0 \text{ V}$

2. Example (when $C_{TP} = 0.1 \mu\text{F}$ and $C_{TW} = 0.01 \mu\text{F}$)

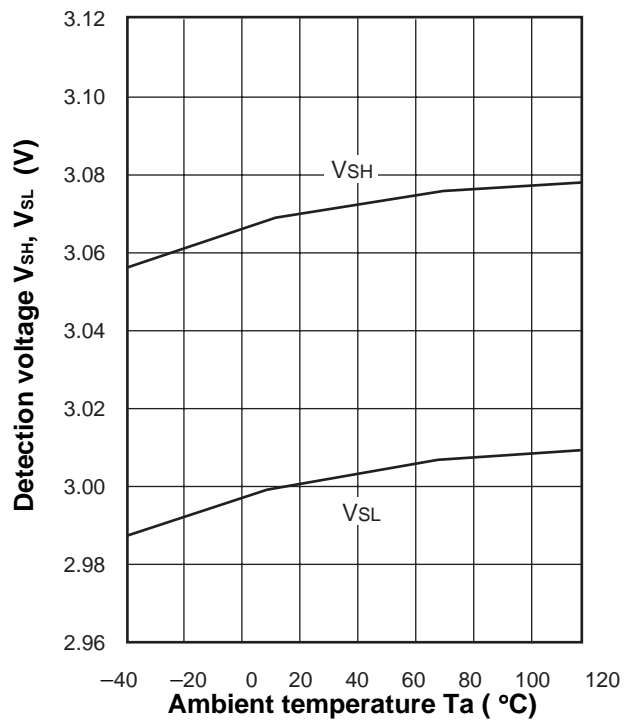
time (ms)	Symbol	V _{CC} = 3.3 V	V _{CC} = 5.0 V
		t_{PR}	75
	t_{WD}	16	15
	t_{WR}	5.5	10

TYPICAL CHARACTERISTICS

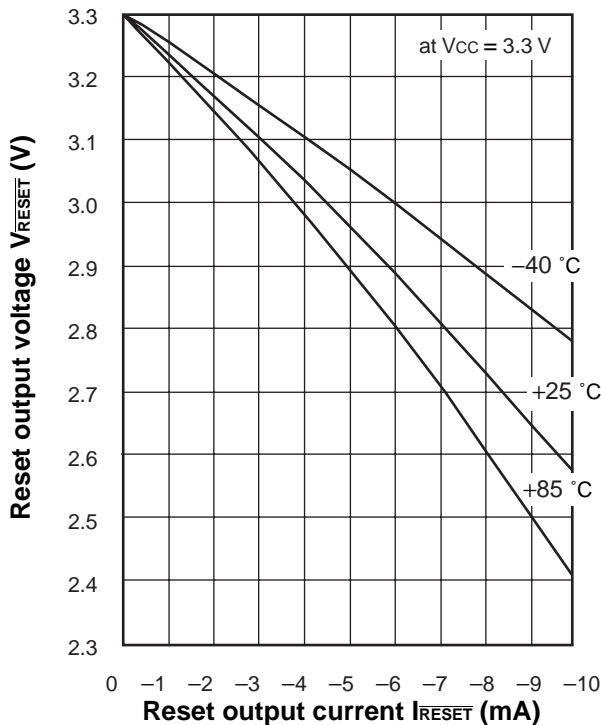
Power supply current vs. power supply voltage



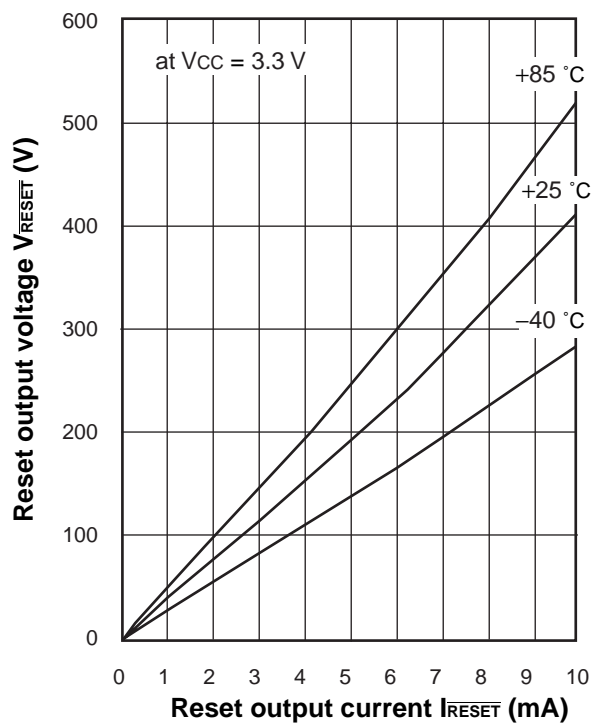
Detection voltage vs. ambient temperature



Reset output voltage vs. reset output current (P-MOS side)



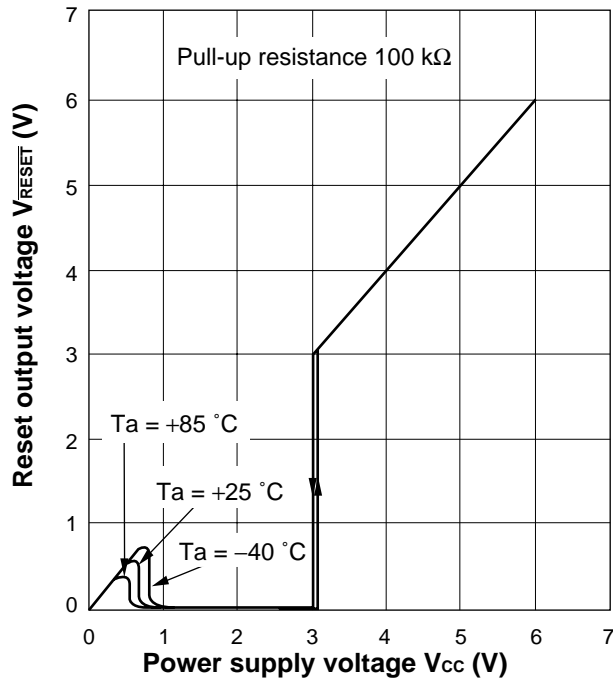
Reset output voltage vs. reset output current (N-MOS side)



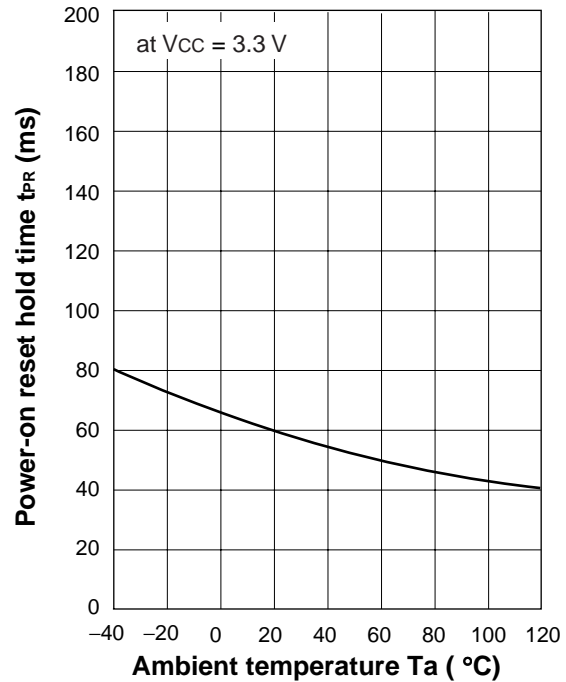
Note : Without writing the value clearly, $V_{CC} = 3.3$ (V), $CTP = 0.1$ (μF), $CTW = 0.01$ (μF).

(Continued)

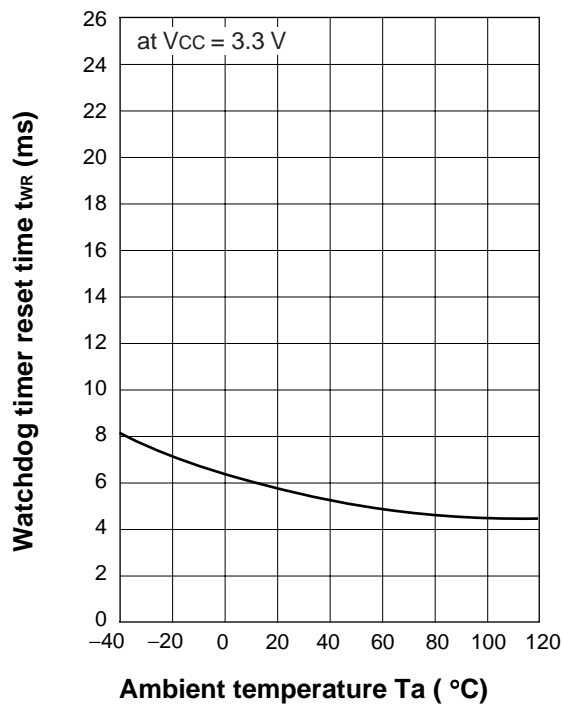
Reset output voltage vs. Power supply voltage



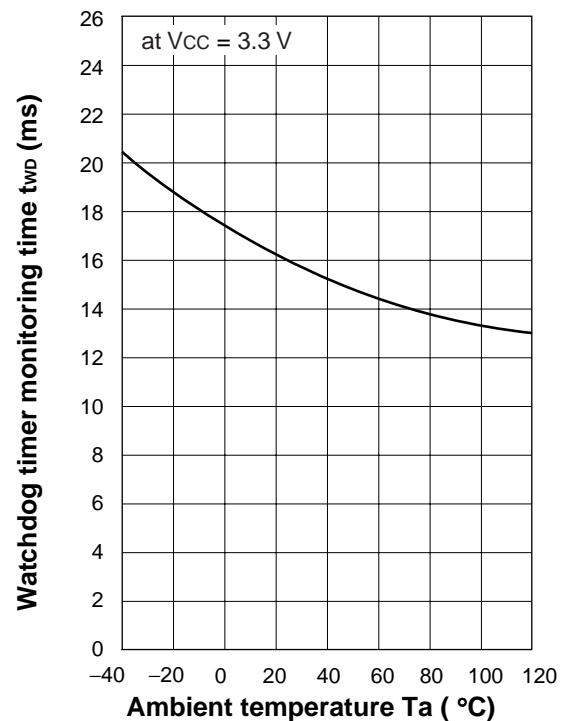
Power-on reset hold time vs. Ambient temperature (When V_{CC} rising)



Watchdog timer reset time vs. Ambient temperature (When monitoring)



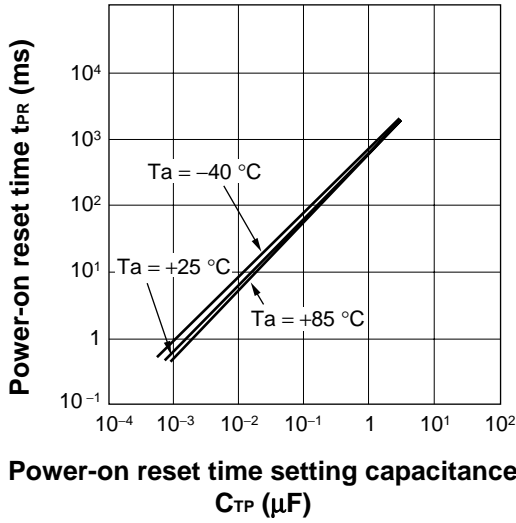
Watchdog timer monitoring time vs. Ambient temperature



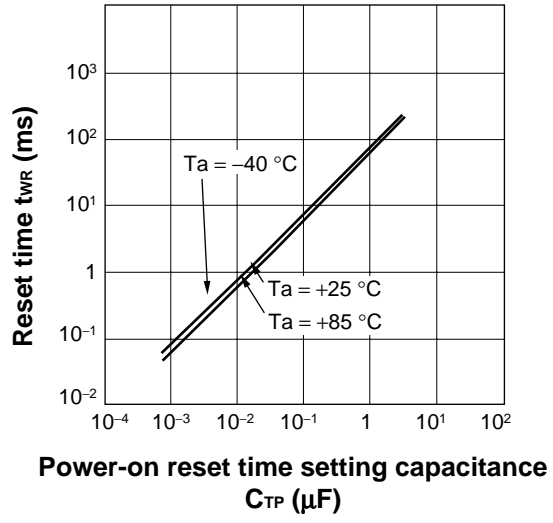
(Continued)

(Continued)

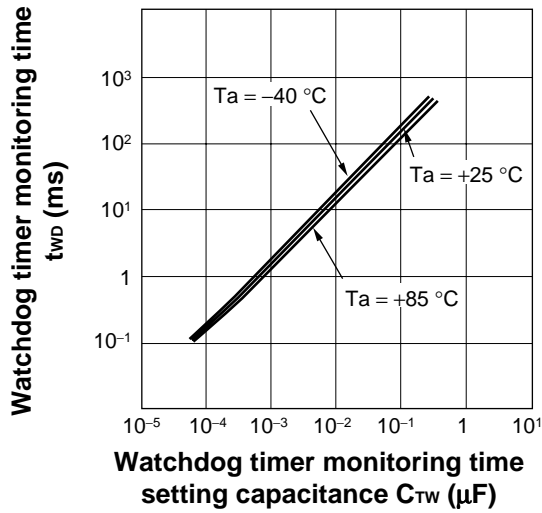
Power-on reset time vs. C_{TP} capacitance



Reset time vs. C_{TP} capacitance

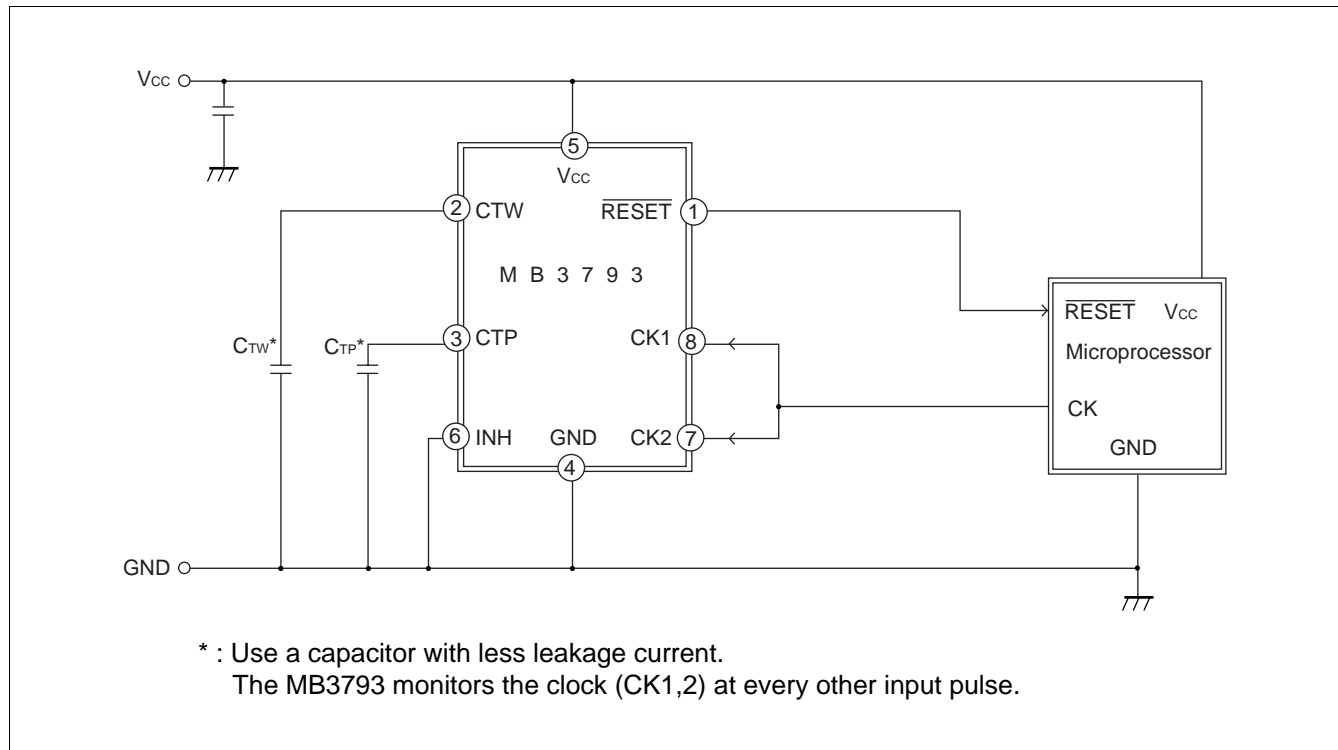


Watchdog timer monitoring time vs. C_{TW} capacitance

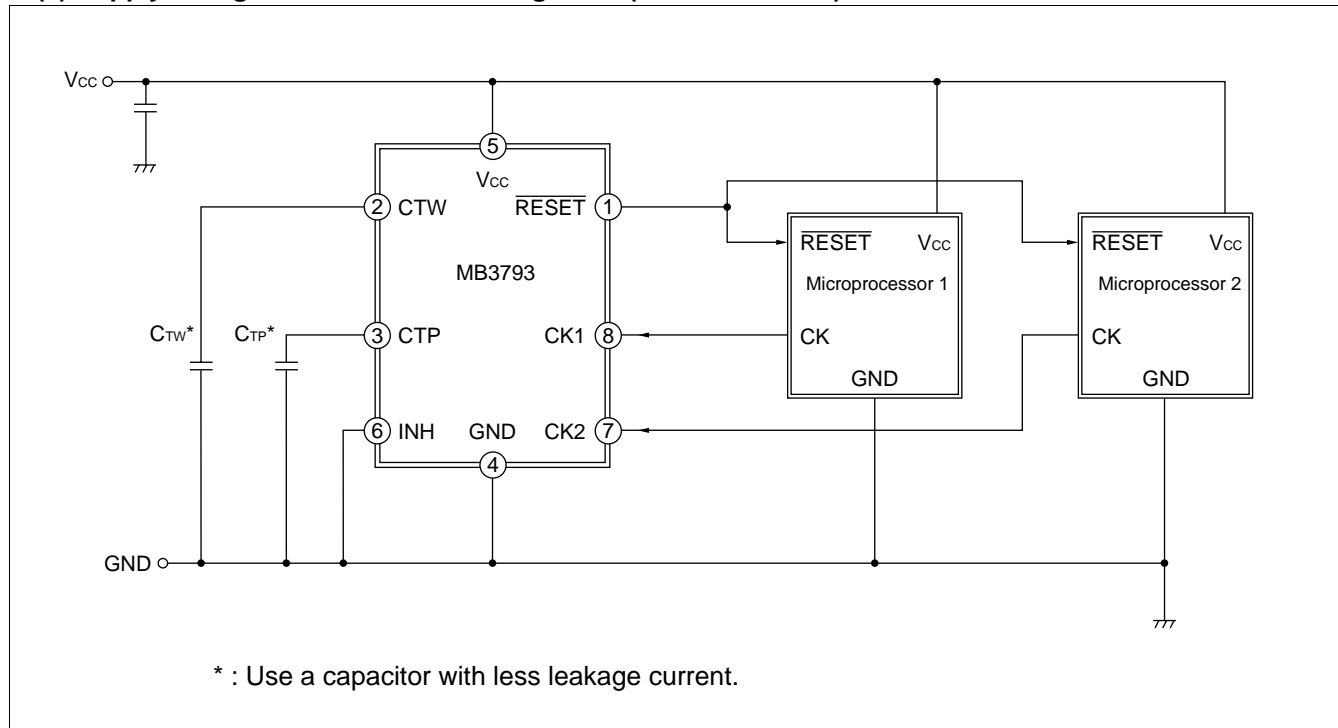


APPLICATION EXAMPLE

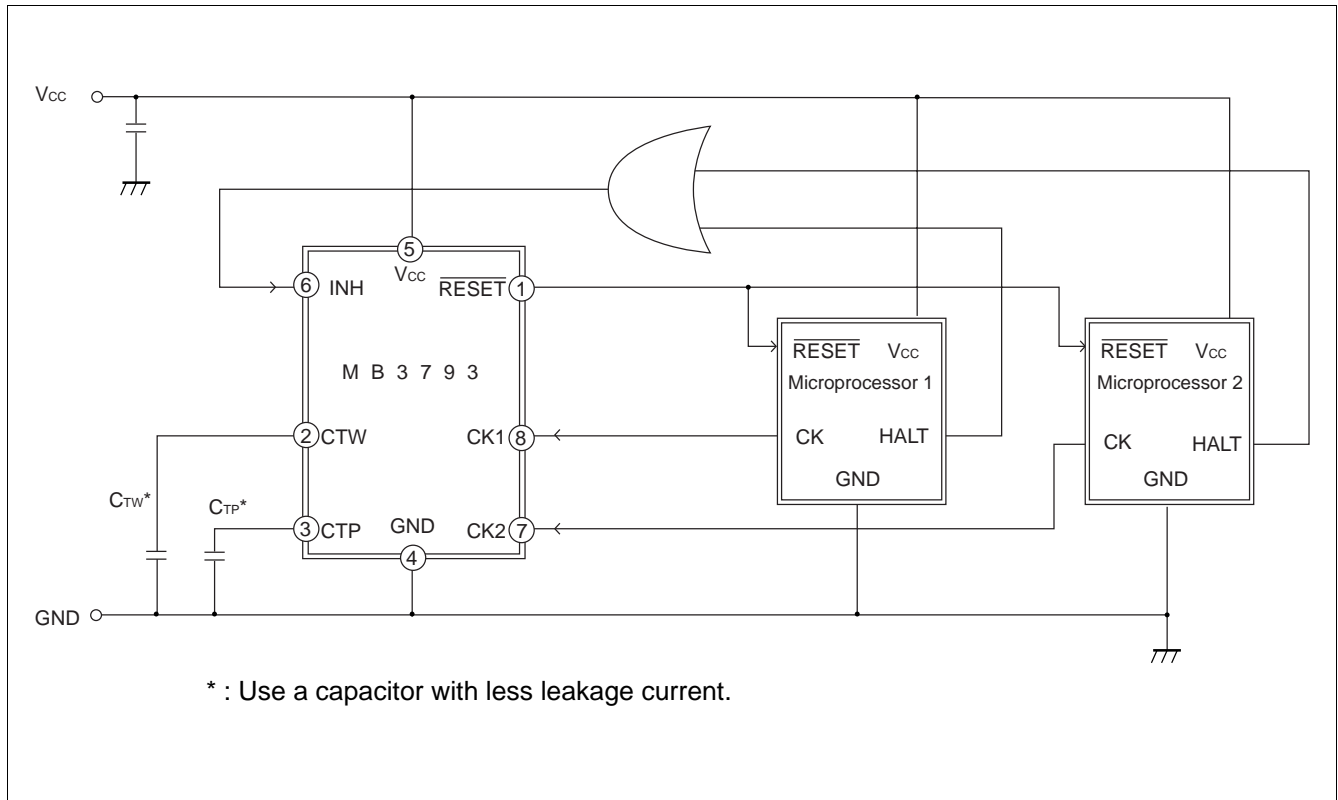
1. (1) Supply voltage monitor and watchdog timer (1-clock monitor)



(2) Supply voltage monitor and watching timer (2-clock monitor)



2. Supply voltage monitor and watchdog timer stop



■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.
- Take measures against static electricity.
 - For semiconductors, use antistatic or conductive containers.
 - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
 - The work table, tools and measuring instruments must be grounded.
 - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.
- Do not apply a negative voltage.
 - Applying a negative voltage of -0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

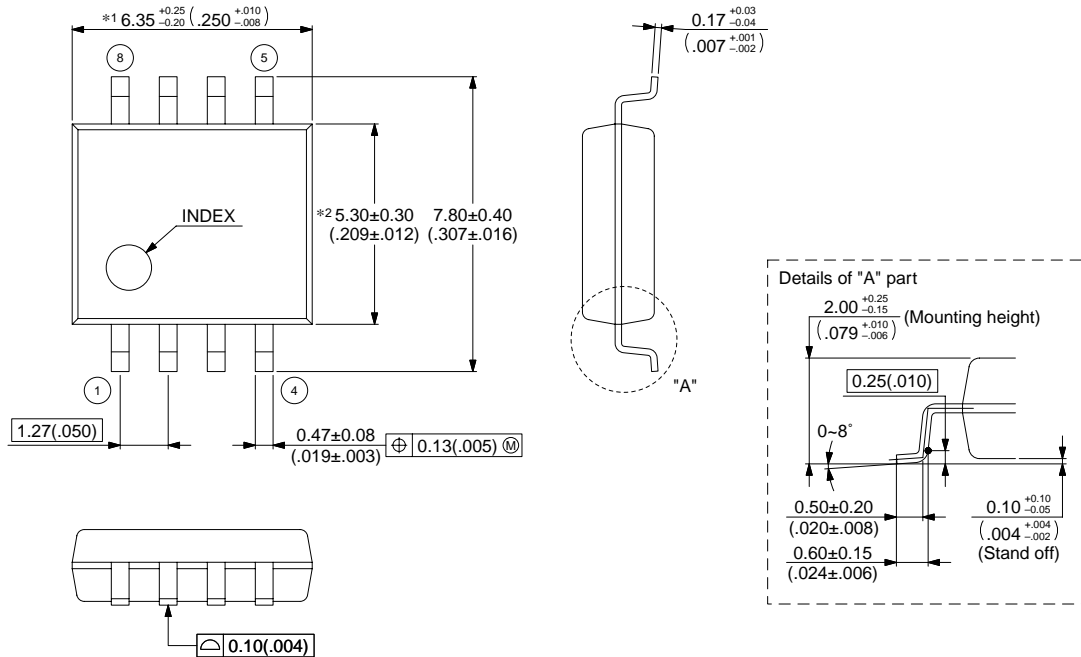
■ ORDERING INFORMATION

Part number	Package	Marking	Remarks
MB3793-30AP	8-pin Plastic DIP (DIP-8P-M01)	3793AN	
MB3793-30APF	8-pin Plastic SOP (FPT-8P-M01)	3793AN	
MB3793-30APNF	8-pin Plastic SOL (FPT-8P-M02)	3793AN	
MB3793-30APFV	8-pin Plastic SSOP (FPT-8P-M03)	93AN	

■ PACKAGE DIMENSIONS

8-pin Plastic SOP (FPT-8P-M01)

- Note 1) *1 : These dimensions include resin protrusion.
 Note 2) *2 : These dimensions do not include resin protrusion.
 Note 3) Pins width and pins thickness include plating thickness.
 Note 4) Pins width do not include tie bar cutting remainder.



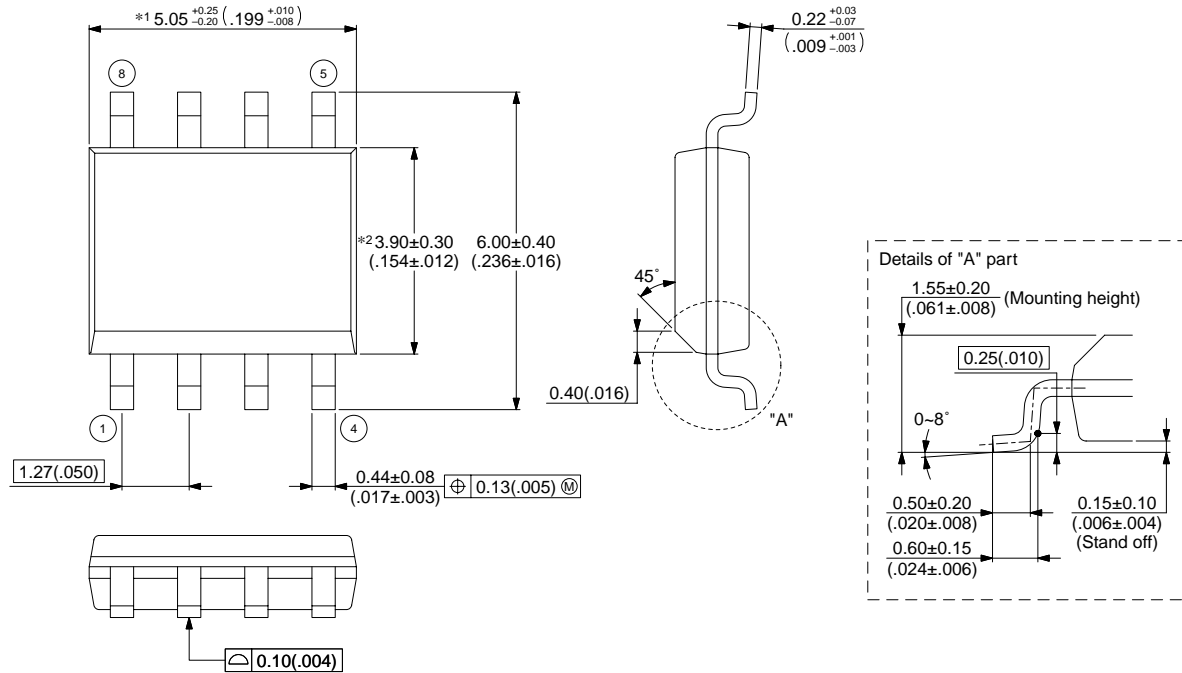
© 2002 FUJITSU LIMITED F08002S-c-6-7

Dimensions in mm (inches) .
 Note : The values in parentheses are reference values.

(Continued)

8-pin Plastic SOP (FPT-8P-M02)

- Note 1) *1 : These dimensions include resin protrusion.
 Note 2) *2 : These dimensions do not include resin protrusion.
 Note 3) Pins width and pins thickness include plating thickness.
 Note 4) Pins width do not include tie bar cutting remainder.



© 2002 FUJITSU LIMITED F08004S-c-4-7

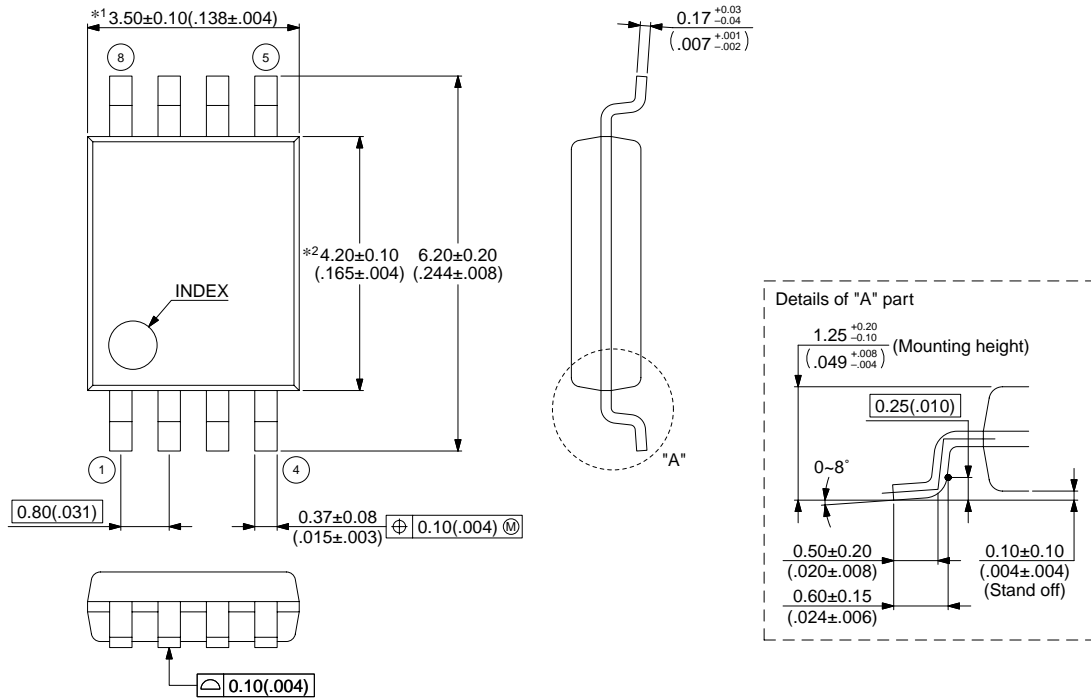
Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

(Continued)

8-pin Plastic SSOP (FPT-8P-M03)

- Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
- Note 2) *2 : These dimensions do not include resin protrusion.
- Note 3) Pins width and pins thickness include plating thickness.
- Note 4) Pins width do not include tie bar cutting remainder.



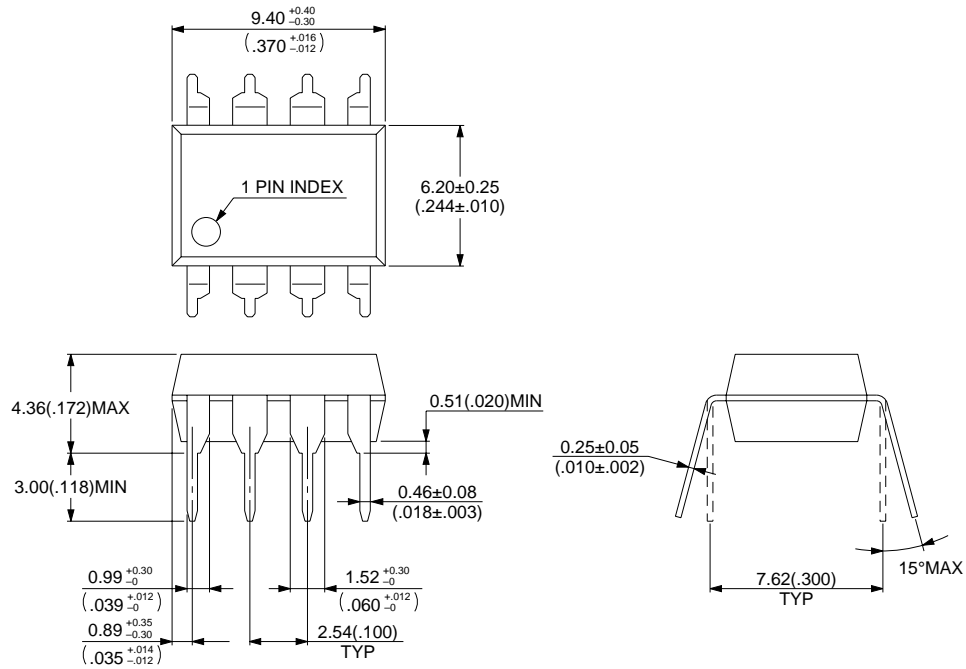
© 2002 FUJITSU LIMITED F08005S-c-3-5

Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

(Continued)

8-pin Plastic DIP (DIP-8P-M01)



© 1994 FUJITSU LIMITED D08006S-2C-3

Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.